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STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS

Technical Field

The technical field relates generally to semiconductor integrated circuits. More particularly, it pertains to capacitors in semiconductor integrated circuits.

Background

A capacitor is composed of two layers of a material that is electrically conductive (hereinafter, electrode) brought near to one another and separated by a material that is electrically nonconductive. Suppose the capacitor is connected to a battery with a certain voltage level (hereinafter, energy level). Charges will flow from the battery to be stored in the capacitor until the capacitor exhibits the energy level of the battery. Then, suppose further that the capacitor is disconnected from the battery. The capacitor will indefinitely exhibit the energy level of the battery until the charges stored in the capacitor are removed either by design or by accident.

This ability of the capacitor to "remember" an energy level is valuable to the operation of semiconductor integrated circuits. Often, the operation of such circuits may require that data be stored and retrieved as desired. Because of its ability to remember, the capacitor is a major component of a semiconductor memory cell. One memory cell may store one bit of data. A system of memory cells is a semiconductor memory array where information can be randomly stored or retrieved from each memory cell. Such a system is also known as a random-access memory.

One type of random-access memory is dynamic random-access memory (DRAM). The charges stored in DRAM tend to leak away over a short time. It is thus necessary to periodically refresh the charges stored in the DRAM by the use of additional circuitry. Even with the refresh burden, DRAM is a popular type of memory because it can occupy a very small space on a semiconductor surface. This

is desirable because of the need to maximize storage capacity on the limited surface area of an integrated circuit

One type of capacitor that supports an increase in storage capacity uses a metal substance as a bottom electrode and an electrically nonconductive material that has a high dielectric constant. The metal substance tends to create undesired atomic diffusion in an environment with a high temperature. Such a high temperature, however, is needed to further process the electrically nonconductive material. The undesired atomic diffusion may act to degrade the electrically nonconductive material. That act compromises the ability of the capacitor to maintain the charges. This is detrimental to the storage ability of the capacitor and would render such a memory cell defective.

Thus, what is needed are systems, devices, structures, and methods to inhibit the described effect so as to enhance capacitors with a high dielectric constant in manufacturing environments exhibiting high temperatures.

Summary

The above-mentioned problems with capacitors as well as other problems are addressed by the present invention and will be understood by reading and studying the following specification. Systems, devices, structures, and methods are described which accord these benefits.

An illustrative embodiment includes a capacitor. The capacitor includes a first electrode, a dielectric having a first compound, and a second electrode having a second compound that includes a third and a fourth substance. The first compound of the dielectric includes a first substance and a second substance. The first compound includes ditantalum pentaoxide. The second electrode also contains a trace amount of the third substance. The second compound in an as-deposited state includes a substantial amount of the fourth substance. The trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion

of at least one of the first substance and the second substance is inhibited. The crystalline structure of the dielectric describes substantially a (001) lattice plane. The second compound includes RuO_x. The x is indicative of a desired number of atoms.

Another illustrative embodiment includes a method for enhancing a semiconductor structure that stores charges. The method includes forming a conductive layer of RuO_x, crystallizing to form RuO_2 and a trace amount of Ru, forming an amorphous insulator layer of Ta_2O_5, and forming a crystallized Ta_2O_5 with a desired lattice plane such that the permittivity of the crystallized Ta_2O_5 is greater than about 25.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

Figure 1 is a cross-sectional view of a semiconductor structure according to one embodiment of the present invention.

Figure 2 is an elevation view of a semiconductor memory array according to one embodiment of the present invention.

Figures 3A-3K are cross-sectional views of a semiconductor structure during processing according to one embodiment of the present invention.

Figure 4 is a block diagram of a device according to one embodiment of the present invention.

Figure 5 is an elevation view of a semiconductor wafer according to one embodiment of the present invention.

Figure 6 is a block diagram of a circuit module according to one embodiment of the present invention.

Figure 7 is a block diagram of a memory module according to one embodiment of the present invention.

Figure 8 is a block diagram of a system according to one embodiment of the present invention.

Figure 9 is a block diagram of a system according to one embodiment of the present invention.

Figure 10 is a block diagram of a system according to one embodiment of the present invention.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when

reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure and layer formed above, and the terms wafer or substrate include the underlying layers containing such regions/junctions and any layer that may have been formed above. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Figure 1 is a cross-sectional view of a semiconductor structure according to one embodiment of the present invention. The semiconductor structure 100 may illustrate an example of a single DRAM cell. The semiconductor structure 100 includes a substrate 102, field isolators 104, transistor 134, insulation layers 120, another semiconductor structure such as a capacitor 136, and a metallization layer 140. In one embodiment, the metallization layer 140 may be considered a conductive plug. In another embodiment, the conductive plug includes polysilicon. The transistor 134 includes source/drain regions 106_0 and 106_1, silicide region 108, spacers 112, gate oxide 114, and gate 116. The source/drain regions 106_0 and 106_1 include lightly doped source/drain regions 110. The capacitor 136 includes an electrode 124, a dielectric layer 126, and another electrode 128. The dielectric layer 126 is coupled to the electrodes 124 and 128.

Charges can be transferred into or removed from the capacitor 136 by turning on the transistor 134. The transistor 134 is turned on by an appropriate voltage level and polarity placed at the gate 116 so that a depletion region and conducting channel are formed between the source/drain regions 106_0 and 106_1. If charges are to be transferred into the capacitor 136, these charges are introduced at the source/drain region 106_0 by a buried bit line 141, so that they may travel across the conducting channel into the source/drain region 106_1, conduct through the metallization layer 140, and enter the electrode 124. The charges cannot go any further because the dielectric layer 126 is electrically nonconductive. However, these charges will attract opposite polarity

charges to appear at electrode 128. Hence, an electric field is set up between the electrodes 124 and 128. Energy is stored in this electric field. This electric field is the phenomenon that allows the capacitor to "remember."

There exists an industry-wide drive to smaller memory cells to increase storage density on the limited surface area of an integrated circuit. This has motivated the use of a thin film nonconductive material for use as a dielectric 126 of the capacitor 136. High temperatures may be used in the processing of the semiconductor structure 100. Such high temperatures may cause the bottom electrode 124 to undesirably act with a portion of the semiconductor structure 100, such as the dielectric 126 of the capacitor 136. Such action may degrade the properties of the dielectric 126 to cause the capacitor 136 to become defective over time.

One example of the degradation of the dielectric 126 includes the use of a metal substance for the bottom electrode 124. A high temperature (about 750 degrees Celsius or greater) is used to crystallize the dielectric 126. At such a high temperature, thermal vibration in the crystal structure of the metal substance increases, thereby increasing the likelihood of structural disruption. Such a structural disruption introduces point defects, such as vacancies in the crystal structure of the metal substance. Suppose that the dielectric 126 includes a compound comprising another metal substance and nonmetal atoms. Under the environment as described above, nonmetal atoms of the dielectric 126 may diffuse to fill the point defects in the crystal structure of the metal substance of the bottom electrode 124. Such a diffusion may short-circuit the capacitor 136. This may occur because the metal substance of the dielectric 126 in the absence of the nonmetal atoms may conductively couple the electrode 124 to the electrode 128.

One solution includes using lower temperatures (750 degrees Celsius or lower) to crystallize the dielectric 126. However, at such temperatures, the dielectric 126 tends to exhibit high leakage values. This may be attributed to insufficient incorporation of the nonmetal atoms with the metal atoms in the crystal structure of the dielectric 126 at low temperatures. Thus, this solution is inadequate.

The embodiments of the present invention solve the above-discussed problem while enhancing the dielectric 126. In one embodiment, a semiconductor structure for storing charges includes an insulator layer having a first compound that includes substances, and a conductive layer having a second compound that includes a first substance and a second substance. The second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer.

In another embodiment, the semiconductor structure includes an insulator layer and a conductive layer having a compound formed from a first substance and a second substance; the conductive layer includes a trace amount of the first substance. The morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the insulator layer.

In another embodiment, the semiconductor structure includes an insulator layer having a permittivity value greater than about 25, and a conductive layer having a compound. The compound remains stable when the insulator layer is crystallized at a high temperature so as to decrease the charge leakage of the insulator layer. In one embodiment, the insulator layer passivates the conductive layer from undesired oxidation.

In another embodiment, the semiconductor structure includes an insulator layer having a permittivity value, and a conductive layer abuttingly coupled to the insulator layer. The crystalline structure of the insulator layer describes a desired lattice plane such that the permittivity value of the insulator layer is greater than about 25. The desired lattice plane includes substantially a (001) plane. In another embodiment, the desired lattice plane is described by three axes; the desired plane is parallel to two of the three axes and intersects one of the three axes.

In another embodiment, the capacitor 136 includes a first electrode, a dielectric that includes ditantalum pentaoxide, and a second electrode having a compound that includes a first substance and a second substance. The compound in an as-deposited

state includes a substantial amount of the second substance so as to inhibit undesired diffusion at a high temperature. The compound includes ruthenium oxide (RuO_x). The x is indicative of a desired number of atoms.

In another embodiment, the capacitor 136 includes a first electrode, a dielectric that includes ditantalum pentaoxide, and a second electrode having a compound that includes a first substance and a second substance. The second electrode includes a trace amount of the first substance. The morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the dielectric. The compound includes RuOx. The x is indicative of a desired number of atoms.

In another embodiment, the capacitor 136 includes a first electrode, a dielectric that includes ditantalum pentaoxide, and a second electrode having a compound. The crystalline structure of the dielectric describes a (001) lattice plane. The compound includes RuOx. The x is indicative of a desired number of atoms.

In another embodiment, the capacitor 136 includes a first electrode, a dielectric having a first compound that includes a first substance and a second substance, and a second electrode having a second compound that includes a third and a fourth substance. The first compound includes ditantalum pentaoxide. The second electrode includes a trace amount of the third substance. The second compound in an as-deposited state includes a substantial amount of the fourth substance. The trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited. The crystalline structure of the dielectric describes substantially a (001) lattice plane. The compound includes RuOx. The x is indicative of a desired number of atoms.

In another embodiment, the capacitor 136 includes a first electrode, a dielectric having a first compound that includes a first substance and a second substance, and a second electrode having a second compound that includes a third substance and a fourth substance. The first electrode has a substance that is selected from a group consisting of

TiN, TiON, WN_x, TaN, Ta, Pt, Pt-Rh, Pt-RhO_x, Ru, RuO_x, Ir, IrO_x, Pt-Ru, Pt-RuO_x, Pt-Ir, Pt-IrO_x, $SrRuO_3$, Au, Pd, Al, Mo, Ag, and Poly-Si. The first compound includes ditantalum pentaoxide. The second electrode includes a trace amount of the third substance. The second compound in an as-deposited state includes a substantial amount of the fourth substance. The trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited. The crystalline structure of the dielectric describes substantially a (001) lattice plane. The second compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

Figure 2 is an elevation view of a semiconductor memory array according to one embodiment of the present invention. The memory array 200 includes memory cell regions 242 formed overlying active areas 250. Active areas 250 are separated by field isolation regions 252. Active areas 250 and field isolation regions 252 are formed overlying a semiconductor substrate.

The memory cell regions 242 are arrayed substantially in rows and columns. Shown in Figure 2 are portions of three rows 201A, 201B and 201C. Separate digit lines (not shown) would be formed overlying each row 201 and coupled to active areas 250 through digit line contact regions 248. Word line regions 244 and 246 are further coupled to active areas 250, with word line regions 244 coupled to active areas 250 in row 201B and word line regions 246 coupled to active areas 250 in rows 201A and 201C. The word line regions 244 and 246, coupled to memory cells in this alternating fashion, generally define the columns of the memory array. This folded bit-line architecture is well known in the art for permitting higher densification of memory cell regions 242.

Figures 3A-3K are cross-sectional views of a semiconductor structure during processing according to one embodiment of the present invention. Figures 3A-3K are cross-sectional views taken along line A-AN of Figure 2 during various processing stages.

Semiconductor structure 300 includes a substrate 302. The substrate 302 may be a silicon substrate, such as a p-type silicon substrate. Field isolators 304 are formed over field isolation regions 352 of the substrate 302. Field isolators 304 are generally formed of an insulator material, such as silicon oxides, silicon nitrides, or silicon oxynitrides. In this embodiment, field isolators 304 are formed of silicon dioxide such as by conventional local oxidation of silicon which creates substantially planar regions of oxide on the substrate surface. Active area 350 is an area not covered by the field isolators 304 on the substrate 302. The creation of the field isolators 304 is preceded or followed by the formation of a gate dielectric layer 314. In this embodiment, gate dielectric layer 314 is a thermally grown silicon dioxide, but other insulator materials may be used as described herein.

The creation of the field isolators 304 and gate dielectric layer 314 is followed by the formation of a conductively doped gate layer 316, silicide layer 308, and gate spacers 312. These layers and spacers are formed by methods well known in the art. The foregoing layers are patterned to form word lines in word line regions 344 and 346. A portion of these word lines is illustratively represented by gates 338_0, 338_1, 338_2, and 338_3. In one embodiment, the silicide layer 308 includes a refractory metal layer over the conductively doped gate layer 316, such as a polysilicon layer.

Source/drain regions 306 are formed on the substrate 302 such as by conductive doping of the substrate. Source/drain regions 306 have a conductivity opposite the substrate 302. For a p-type substrate, source/drain regions 306 would have an n-type conductivity. The source/drain regions 306 include lightly doped source/drain regions 310 that are formed by implanting a low-dose substance, such as an n-type or p-type material. Such lightly doped source/drain regions 310 help to reduce high field in the source/drain junctions of a small-geometry semiconductor structure, such as semiconductor structure 300. In one embodiment, each of the gates 338_0, 338_1, 338_2, and 338_3 is enclosed by a nitride compound layer. The nitride compound layer includes a molecular formula of Si_xN_y. The variables x and y are indicative of a desired number

of atoms. The portion of the word lines that are illustratively represented by gates 338_0, 338_1, 338_2, and 338_3 is adapted to be coupled to periphery contacts (not shown). The periphery contacts are located at the end of a memory array and are adapted for electrical communication with external circuitry.

The foregoing discussion is illustrative of one example of a portion of a fabrication process to be used in conjunction with the various embodiments of the invention. Other methods of fabrication are also feasible and perhaps equally viable. For clarity purposes, many of the reference numbers are eliminated from subsequent drawings so as to focus on the portion of interest of the semiconductor structure 300.

Figure 3B shows the semiconductor structure following the next sequence of processing. A thick insulation layer 320 is deposited overlying substrate 302 as well as field isolation regions 352 and active regions 350. Insulation layer 320 is an insulator material such as silicon oxide, silicon nitride, and silicon oxynitride. In one embodiment, insulation layer 320 is a doped insulator material such as borophosphosilicate glass (BPSG), a boron and phosphorous-doped silicon oxide. The insulation layer 320 is planarized, such as by chemical-mechanical planarization (CMP), in order to provide a uniform height.

Figure 3C shows the semiconductor structure following the next sequence of processing. The first inhibiting layer 330_0 is optionally formed on or abutting the insulation layer 320. The first inhibiting layer 330_0 includes a nitride compound. In one embodiment, the first inhibiting layer 330_0 includes a metal nitride compound. The nitride compound includes a substance with a molecular formula of Si_xN_y. The variables x and y are indicative of the desired number of atoms.

The first inhibiting layer 330_0 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. In this embodiment, the first inhibiting layer 330_0 is patterned to form the first inhibiting layer of a semiconductor structure of interest, such as a capacitor.

Figure 3D shows the semiconductor structure following the next sequence of

processing. The semiconductor structure 300 is patterned using photolithography with appropriately placed masks to define future locations of memory cells. Then portions of the first inhibiting layer 330_0 and the insulation layer 320 are exposed and removed along with the masks. These portions of the first inhibiting layer 330_0 and the insulation layer 320 may be removed by etching or other suitable removal techniques known in the art. Removal techniques are generally dependent on the material of construction of the layer to be removed as well as the surrounding layers to be retained. Patterning of the first inhibiting layer 330_0 and the insulation layer 320 creates openings having bottom portions exposed to portions of the silicide region 308 and sidewalls defined by the insulation layer 320. A metallization layer 340 is formed on the silicide region 308 using a suitable deposition technique. In one embodiment, the metallization layer 340 may be considered a conductive plug. In another embodiment, the conductive plug includes conductive polysilicon.

Figure 3E shows the semiconductor structure following the next sequence of processing. A second inhibiting layer 330_1 is optionally formed on the first inhibiting layer 330_0, the insulation layer 320, and the metallization layer 340. The second inhibiting layer 330_1 includes a nitride compound. In one embodiment, the second inhibiting layer 330_1 includes a metal nitride compound. The nitride compound includes a substance with a molecular formula of Si_xN_y. The variables x and y are indicative of the desired number of atoms. The second inhibiting layer 330_1 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques.

Figure 3F shows the semiconductor structure following the next sequence of processing. In one embodiment, the second inhibiting layer 330_1 is etched to define a chamber with an aperture that adjoins the metallization layer 340 and two sidewalls extending outwardly from the aperture. In one embodiment, the etching technique is selected from a group consisting of a spacer etching technique and an etch-back technique.

Figure 3G shows the semiconductor structure following the next sequence of processing. A conductive layer 324 is formed on or adjoining to the inhibiting layer 330_0, the insulation layer 320 and the metallization layer 340. The conductive layer 324 includes a conductive material. In one embodiment, the conductive material includes an as-deposited film of a conductive compound. The conductive compound includes a first substance and a substantial amount of a second substance. The first substance includes ruthenium. The second substance includes oxygen. The conductive compound includes RuO_x. The x is indicative of a desired number of atoms.

The conductive layer 324 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. In this embodiment, the conductive layer 324 forms the bottom conductive layer, or bottom electrode, or bottom plate of a semiconductor structure of interest, such as a capacitor.

In one embodiment, the conductive layer 324 is formed in about 210 degrees Celsius. In another embodiment, the first substance includes about 200 sccm of Ru-HEC. In another embodiment, the second substance includes about 250 sccm of O_2. In another embodiment, the conductive layer 324 is formed in about 2.5 torrs.

After the formation of the conductive layer 324, in one embodiment, the conductive layer 324 undergoes an act of crystallizing to form a crystallized film. In one embodiment, the act of crystallizing occurs at a temperature that is greater than about 750 degrees Celsius and less than about 800 degrees Celsius. In another embodiment, the act of crystallizing occurs in an ambient of nitrogen. In another embodiment, the act of crystallizing results in compounds and substances that include ruthenium dioxide and a trace amount of ruthenium.

The conductive layer 324 may undergo a localizing or a polishing process such as by a chemical mechanical planarization technique or other suitable techniques. Such a localizing technique disposes the conductive layer 324 to adjoin the metallization layer 340. In another embodiment, the conductive layer 324 undergoes an etching process such as by a wet etch technique or a dry etch technique. The result is as shown

in Figure 3G.

Figure 3H shows the semiconductor structure following the next sequence of processing. An insulator layer (or dielectric layer) 326 is formed on or adjoining the first inhibiting layer 330_0, the second inhibiting layer 330_1, and the conductive layer 324. The dielectric layer 326 includes an oxide compound. In one embodiment, the dielectric layer 326 is a thin film dielectric. In one embodiment, the oxide compound includes ditantalum pentaoxide. In another embodiment, the dielectric layer 326 includes a thin film of a high permittivity insulator material. In another embodiment, the dielectric layer 326 includes an amorphous insulator layer. The dielectric layer 326 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques.

After the formation of the dielectric layer 326, in one embodiment, the dielectric layer 326 undergoes an act of crystallizing to form crystallized Ta_2O_5. The act of crystallizing to form crystallized Ta_2O_5 converts a trace amount of ruthenium that may remain from the formation of the conductive layer 324. Such conversion includes converting the trace amount of ruthenium into ruthenium dioxide. In one embodiment, the act of crystallizing occurs at a temperature of about 800 degrees Celsius. In another embodiment, the act of crystallizing occurs in an ambient of dinitrogen oxide. In another embodiment, the act of crystallizing occurs in an ambient of oxygen.

In one embodiment, the act of crystallizing forms a crystallized Ta_2O_5 with a desired lattice plane such that the permittivity of the crystallized Ta_2O_5 is greater than about 25. The desired lattice plane includes substantially a (001) lattice plane.

Figure 3I shows the semiconductor structure following the next sequence of processing. A conductive layer 328 is formed on the dielectric layer 326. The conductive layer 328 includes a conductive material. The conductive layer 328 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. In this embodiment, the conductive layer 328 forms the top conductive layer, or top electrode, or top plate of a semiconductor

structure of interest, such as a capacitor.

A third inhibiting layer 330_2 is optionally formed on the conductive layer 328. The third inhibiting layer 330_2 includes a nitride compound. In one embodiment, the third inhibiting layer 330_2 includes a metal nitride compound. The nitride compound includes a substance with a molecular formula of Si_xN_y. The variables x and y are indicative of the desired number of atoms. The third inhibiting layer 330_2 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques.

Figure 3J shows the semiconductor structure following the next sequence of processing. The semiconductor structure 300 is patterned using photolithography with appropriately placed masks to define a number of capacitors to be used in memory cells. Then portions of the first inhibiting layer 330_0, the dielectric layer 326, the conductive layer 328, and the second inhibiting layer 330_2 are exposed and removed along with the masks. Those of the first inhibiting layer 330_0, the dielectric layer 326, the conductive layer 328, and the second inhibiting layer 330_2 may be removed by etching or other suitable removal techniques known in the art. Removal techniques are generally dependent on the material of construction of the layer to be removed as well as the surrounding layers to be retained. Patterning of the first inhibiting layer 330_0, the dielectric layer 326, the conductive layer 328, and the second inhibiting layer 330_2 defines two edges or terminals for each capacitor 336_0 and 336_1. These edges are the result of etching the various portions of the semiconductor structure 300 down to the insulation layer 320.

Figure 3K shows the semiconductor structure following the next sequence of processing. A fourth inhibiting layer 330_3 is optionally formed on the insulator layer 320 and the capacitors 336_0 and 336_1. The fourth inhibiting layer 330_3 includes a nitride compound. In one embodiment, the fourth inhibiting layer 330_3 includes a metal nitride compound. The nitride compound includes a substance with a molecular formula of Si_xN_y. The variables x and y are indicative of the desired number of atoms. The fourth

inhibiting layer 330_3 may be formed by any method, such as collimated sputtering, chemical vapor deposition (CVD), or other deposition techniques. Once the fourth inhibiting layer 330_3 is formed, a portion of the fourth inhibiting layer 330_3 is removed using a suitable technique, such as reactive ion etching. Such etching defines sidewall spacers as shown in Figure 3J.

A digit line contact 341 is formed over the digit line contact regions 348. The formation of the digit line contact 341 and the completion of the semiconductor structure 300 do not limit the embodiments of the present invention and as such will not be discussed here in detail.

Figure 4 is a block diagram of a device according to one embodiment of the present invention. The memory device 400 includes an array of memory cells 402, address decoder 404, row access circuitry 406, column access circuitry 408, control circuitry 410, and input/output circuit 412. The memory device 400 can be coupled to an external microprocessor 414, or memory controller for memory accessing. The memory device 400 receives control signals from the processor 414, such as WE*, RAS*, and CAS* signals. The memory device 400 is used to store data which is accessed via I/O lines. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device 400 has been simplified to help focus on the invention. At least one of the memory cells includes a semiconductor structure in accordance with the aforementioned embodiments.

It will be understood that the above description of a DRAM (Dynamic Random Access Memory) is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a DRAM. Further, the invention is equally applicable to any size and type of memory circuit and is not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic

Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging memory technologies.

As recognized by those skilled in the art, memory devices of the type described herein are generally fabricated as an integrated circuit containing a variety of semiconductor devices. The integrated circuit is supported by a substrate. Integrated circuits are typically repeated multiple times on each substrate. The substrate is further processed to separate the integrated circuits into dies as is well known in the art.

Figure 5 is an elevation view of a semiconductor wafer according to one embodiment of the present invention. In one embodiment, a semiconductor die 510 is produced from a wafer 500. A die is an individual pattern, typically rectangular, on a substrate that contains circuitry, or integrated circuit devices, to perform a specific function. At least one of the integrated circuit devices includes a memory cell that includes a semiconductor structure as discussed in the various embodiments heretofore in accordance with the invention. A semiconductor wafer will typically contain a repeated pattern of such dies containing the same functionality. Die 510 may contain circuitry for the inventive memory device, as discussed above. Die 510 may further contain additional circuitry to extend to such complex devices as a monolithic processor with multiple functionality. Die 510 is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for unilateral or bilateral communication and control.

Figure 6 is a block diagram of a circuit module according to one embodiment of the present invention. Two or more dies 610 may be combined, with or without protective casing, into a circuit module 600 to enhance or extend the functionality of an individual die 610. Circuit module 600 may be a combination of dies 610 representing a variety of functions, or a combination of dies 610 containing

the same functionality. One or more dies 610 of circuit module 600 contain at least one semiconductor structure in accordance with the embodiments of the present invention.

Some examples of a circuit module include memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Circuit module 600 may be a subcomponent of a variety of electronic systems, such as a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and others. Circuit module 600 will have a variety of leads 612 extending therefrom and coupled to the dies 610 providing unilateral or bilateral communication and control.

Figure 7 is a block diagram of a memory module according to one embodiment of the present invention. Memory module 700 contains multiple memory devices 710 contained on support 715, the number depending upon the desired bus width and the desire for parity. Memory module 700 accepts a command signal from an external controller (not shown) on a command link 720 and provides for data input and data output on data links 730. The command link 720 and data links 730 are connected to leads 740 extending from the support 715. Leads 740 are shown for conceptual purposes and are not limited to the positions as shown. At least one of the memory devices 710 includes a memory cell that includes a semiconductor structure as discussed in various embodiments in accordance with the invention.

Figure 8 is a block diagram of a system according to one embodiment of the present invention. Electronic system 800 contains one or more circuit modules 802. Electronic system 800 generally contains a user interface 804. User interface 804 provides a user of the electronic system 800 with some form of control or observation of the results of the electronic system 800. Some examples of user interface 804 include the keyboard, pointing device, monitor, or printer of a personal

computer; the tuning dial, display, or speakers of a radio; the ignition switch, gauges, or gas pedal of an automobile; and the card reader, keypad, display, or currency dispenser of an automated teller machine. User interface 804 may further describe access ports provided to electronic system 800. Access ports are used to connect an electronic system to the more tangible user interface components previously exemplified. One or more of the circuit modules 802 may be a processor providing some form of manipulation, control, or direction of inputs from or outputs to user interface 804, or of other information either preprogrammed into, or otherwise provided to, electronic system 800. As will be apparent from the lists of examples previously given, electronic system 800 will often contain certain mechanical components (not shown) in addition to circuit modules 802 and user interface 804. It will be appreciated that the one or more circuit modules 802 in electronic system 800 can be replaced by a single integrated circuit. Furthermore, electronic system 800 may be a subcomponent of a larger electronic system. At least one of the circuit modules 802 includes a memory cell that includes a semiconductor structure as discussed in various embodiments in accordance with the invention.

Figure 9 is a block diagram of a system according to one embodiment of the present invention. Memory system 900 contains one or more memory modules 902 and a memory controller 912. Each memory module 902 includes at least one memory device 910. Memory controller 912 provides and controls a bidirectional interface between memory system 900 and an external system bus 920. Memory system 900 accepts a command signal from the external bus 920 and relays it to the one or more memory modules 902 on a command link 930. Memory system 900 provides for data input and data output between the one or more memory modules 902 and external system bus 920 on data links 940. At least one of the memory devices 910 includes a memory cell that includes a semiconductor structure as discussed in various embodiments in accordance with the invention.

Figure 10 is a block diagram of a system according to one embodiment of the present invention. Computer system 1000 contains a processor 1010 and a memory system 1002 housed in a computer unit 1005. Computer system 1000 is but one example of an electronic system containing another electronic system, e.g., memory system 1002, as a subcomponent. The memory system 1002 may include a memory cell that includes a semiconductor structure as discussed in various embodiments of the present invention. Computer system 1000 optionally contains user interface components. These user interface components include a keyboard 1020, a pointing device 1030, a monitor 1040, a printer 1050, and a bulk storage device 1060. It will be appreciated that other components are often associated with computer system 1000 such as modems, device driver cards, additional storage devices, etc. It will further be appreciated that the processor 1010 and memory system 1002 of computer system 1000 can be incorporated on a single integrated circuit. Such single-package processing units reduce the communication time between the processor and the memory circuit.

Conclusion

Systems, devices, structures, and methods have been described to address situations where, at high temperature, undesired diffusion acts against a high permittivity dielectric in a capacitor such that degradation occurs. Capacitors that are formed using at least one technique as described heretofore benefit from the dual ability of having an increase in storage capability yet maintain reliability in the process of manufacturing involving high temperatures.

Although the specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the

above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention includes any other applications in which the above structures and fabrication methods are used. Accordingly, the scope of the invention should only be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

We claim:

1. A semiconductor structure for storing charges, comprising:

an insulator layer having a first compound that includes substances; and

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer.

2. The semiconductor structure of claim 1, wherein the first compound includes ditantalum pentaoxide.

3. The semiconductor structure of claim 1, wherein the first substance includes ruthenium atoms.

4. The semiconductor structure of claim 1, wherein the second substance includes oxygen atoms.

5. The semiconductor structure of claim 1, wherein the second compound includes RuO_x, wherein x is indicative of a desired number of atoms.

6. A semiconductor structure for storing charges, comprising:

an insulator layer; and

a conductive layer having a compound formed from a first substance and a second substance, wherein the conductive layer includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the insulator layer.

7. The semiconductor structure of claim 6, wherein the compound includes RuO_x, wherein x is indicative of a desired number of atoms.

8. The semiconductor structure of claim 6, wherein the first substance includes ruthenium.

9. The semiconductor structure of claim 6, wherein the second substance includes oxygen.

10. The semiconductor structure of claim 6, wherein the insulator layer includes ditantalum pentaoxide.

11. A semiconductor structure for storing charges, comprising:

an insulator layer having a permittivity value greater than about 25; and

a conductive layer having a compound, wherein the compound remains stable when the insulator layer is crystallized at a high temperature so as to decrease the charge leakage of the insulator layer.

12. The semiconductor structure of claim 11, wherein the insulator layer includes ditantalum pentaoxide.

13. The semiconductor structure of claim 11, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

14. The semiconductor structure of claim 11, wherein the high temperature includes greater than about 750 degrees Celsius to less than about 801 degrees Celsius.

15. The semiconductor structure of claim 11, wherein the conductive layer passivates the insulator layer from undesired oxidation.

16. A semiconductor structure for storing charges, comprising:

an insulator layer having a permittivity value; and

a conductive layer abuttingly coupled to the insulator layer, wherein the crystalline structure of the insulator layer describes a desired lattice plane such that the permittivity value of the insulator layer is greater than about 25.

17. The semiconductor structure of claim 16, wherein the insulator layer includes ditantalum pentaoxide.

18. The semiconductor structure of claim 16, wherein the conductive layer includes RuO_x, wherein the x indicates a desired number of atoms.

19. The semiconductor structure of claim 16, wherein the desired lattice plane includes substantially a (001) plane.

20. The semiconductor structure of claim 16, wherein the desired lattice plane is described by three axes, wherein the desired lattice plane is parallel to two of the three axes and intersects one of the three axes.

21. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound that includes a first substance and a

second substance, wherein the compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion at a high temperature, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

22. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound that includes a first substance and a second substance, wherein the second electrode includes a trace amount of the first substance, wherein the morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the dielectric, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

23. A capacitor comprising:

a first electrode;

a dielectric that includes ditantalum pentaoxide; and

a second electrode having a compound, wherein the crystalline structure of the dielectric describes a (001) lattice plane, wherein the compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

24. A capacitor comprising:

a first electrode;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second electrode having a second compound that includes a third substance and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

25. A capacitor comprising:

a first electrode having a substance that is selected from a group consisting of TiN, TiON, WN_x, TaN, Ta, Pt, Pt-Rh, Pt-RhO_x, Ru, RuO_x, Ir, IrO_x, Pt-Ru, Pt-RuO_x, Pt-Ir, Pt-IrO_x, $SrRuO_3$, Au, Pd, Al, Mo, Ag, and Poly-Si;

a dielectric having a first compound that includes a first substance and a second substance, wherein the first compound includes ditantalum pentaoxide; and

a second electrode having a second compound that includes a third substance

and a fourth substance, wherein the second electrode includes a trace amount of the third substance, wherein the second compound in an as-deposited state includes a substantial amount of the fourth substance, wherein the trace amount of the third substance is oxidized during the crystallization of the dielectric such that a diffusion of at least one of the first substance and the second substance is inhibited, wherein the crystalline structure of the dielectric describes substantially a (001) lattice plane, and wherein the second compound includes RuO_x, wherein the x is indicative of a desired number of atoms.

26. A method for enhancing a dielectric, comprising:

forming an as-deposited film of a conductive compound that includes a first substance and a second substance, wherein the act of forming incorporates a substantial amount of the second substance in the as-deposited film so as to inhibit undesired oxidation of the first substance at a high temperature; and

forming the dielectric over the conductive compound.

27. The method of claim 26, wherein the first substance includes ruthenium.

28. The method of claim 26, wherein the second substance includes oxygen.

29. The method of claim 26, wherein the conductive compound includes RuO_x,

wherein the x is indicative of a desired number of atoms.

30. The method of claim 26, wherein the dielectric includes ditantalum pentaoxide.

31. A method for enhancing a semiconductor structure that stores charges, comprising:

forming an as-deposited film of a conductive compound that includes a first substance and a substantial amount of a second substance so as to inhibit volatile oxide states caused by the first substance; and

forming the dielectric over the conductive compound.

32. The method of claim 31, wherein forming includes forming in about 210 degrees Celsius.

33. The method of claim 31, wherein forming includes forming with a first substance, wherein the first substance includes about 200 sccm of Ru-HEC.

34. The method of claim 31, wherein forming includes forming with a second substance, wherein the second substance includes about 250 sccm of O_2.

35. The method of claim 31, wherein forming includes forming at a pressure of about 2.5 torrs.

36. A method for enhancing a semiconductor structure that stores charges, comprising:

forming an as-deposited film of ruthenium oxide that includes a substantial amount of oxygen so as to inhibit morphological change caused by oxidation of ruthenium;

crystallizing the as-deposited film to form a crystallized film; and

forming the dielectric over the crystallized film.

37. The method of claim 36, wherein crystallizing includes crystallizing at a temperature that is greater than about 750 degrees Celsius and less than about 800 degrees Celsius.

38. The method of claim 36, wherein crystallizing includes crystallizing in an ambient of nitrogen.

39. The method of claim 36, wherein the act of crystallizing results in compounds and substances that include ruthenium dioxide and a trace amount of ruthenium.

40. The method of claim 36, wherein forming the as-deposited film depositing the as-deposited film using a technique of chemical vapor deposition.

41. A method for enhancing a semiconductor structure that stores charges, comprising:

forming a conductive layer of RuO_x;

crystallizing to form RuO_2 and a trace amount of Ru;

forming an amorphous insulator layer of Ta_2O_5; and

crystallizing to form crystallized Ta_2O_5, wherein the act of crystallizing to form crystallized Ta_2O_5 converts the trace amount of Ru into RuO_2.

42. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing at a temperature of about 800 degrees Celsius.

43. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing in an ambient of dinitrogen oxide.

44. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 includes crystallizing in an ambient of oxygen.

45. The method of claim 41, wherein crystallizing to form crystallized Ta_2O_5 acts to passivate the conductive layer from volatility caused by the trace amount of Ru.

46. A method for enhancing a semiconductor structure that stores charges, comprising:

forming a conductive layer of RuO_x;

crystallizing to form RuO_2 and a trace amount of Ru;

forming an amorphous insulator layer of Ta_2O_5; and

forming a crystallized Ta_2O_5 with a desired lattice plane such that the permittivity of the crystallized Ta_2O_5 is greater than about 25.

47. The method of claim 46, wherein forming a crystallized Ta_2O_5 includes forming substantially a (001) lattice plane.

48. The method of claim 46, wherein forming a conductive layer of RuO_x includes forming with a substantial amount of oxygen.

49. The method of claim 46, wherein crystallizing includes crystallizing at a temperature of greater than about 750 degrees Celsius to less than about 800 degrees Celsius.

50. The method of claim 46, wherein forming a crystallized Ta_2O_5 includes forming at a temperature of about 800 degrees Celsius.

51. A memory device comprising:

an array of memory cells, wherein the array includes at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

an address decoder;

a row access circuitry;

a column access circuitry;

a controller; and

an input/output circuit.

52. An electronic system comprising:

a plurality of circuit modules includes a plurality of dies, wherein at least one die includes at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired diffusion of at least one substance of the first compound from the insulator layer;

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of leads coupled to the plurality of dies to provide unilateral or bilateral communication and control; and

a user interface.

53. A computer system comprising:

a processor;

a memory system that comprises a plurality of memory modules, wherein one of the plurality of memory modules comprises a plurality of memory devices, wherein at least one memory device comprises at least one array of memory cells, wherein the array comprises at least one capacitor that includes:

an insulator layer having a first compound that includes substances;

a conductive layer having a second compound that includes a first substance and a second substance, wherein the second compound in an as-deposited state includes a substantial amount of the second substance so as to inhibit undesired

diffusion of at least one substance of the first compound from the insulator layer; and

at least one transistor having a gate, drain, and source, wherein the drain is coupled to the second conductive layer;

a plurality of command links coupled to the plurality of memory devices to communicate at least one command signal;

a plurality of data links coupled to the plurality of memory devices to communicate data;

a memory controller;

at least one user interface device, wherein the at least one user interface device includes a monitor;

at least one output device, wherein the at least one output device includes a printer; and

at least one bulk storage device.

STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS

Abstract of the Disclosure

Systems, devices, structures, and methods are described that inhibit dielectric degradation at high temperatures. An enhanced capacitor is discussed. The enhanced capacitor includes a first electrode, a dielectric that includes ditantalum pentaoxide, and a second electrode having a compound. The compound includes a first substance and a second substance. The second electrode includes a trace amount of the first substance. The morphology of the semiconductor structure remains stable when the trace amount of the first substance is oxidized during crystallization of the dielectric. In one embodiment, the crystalline structure of the dielectric describes substantially a (001) lattice plane.

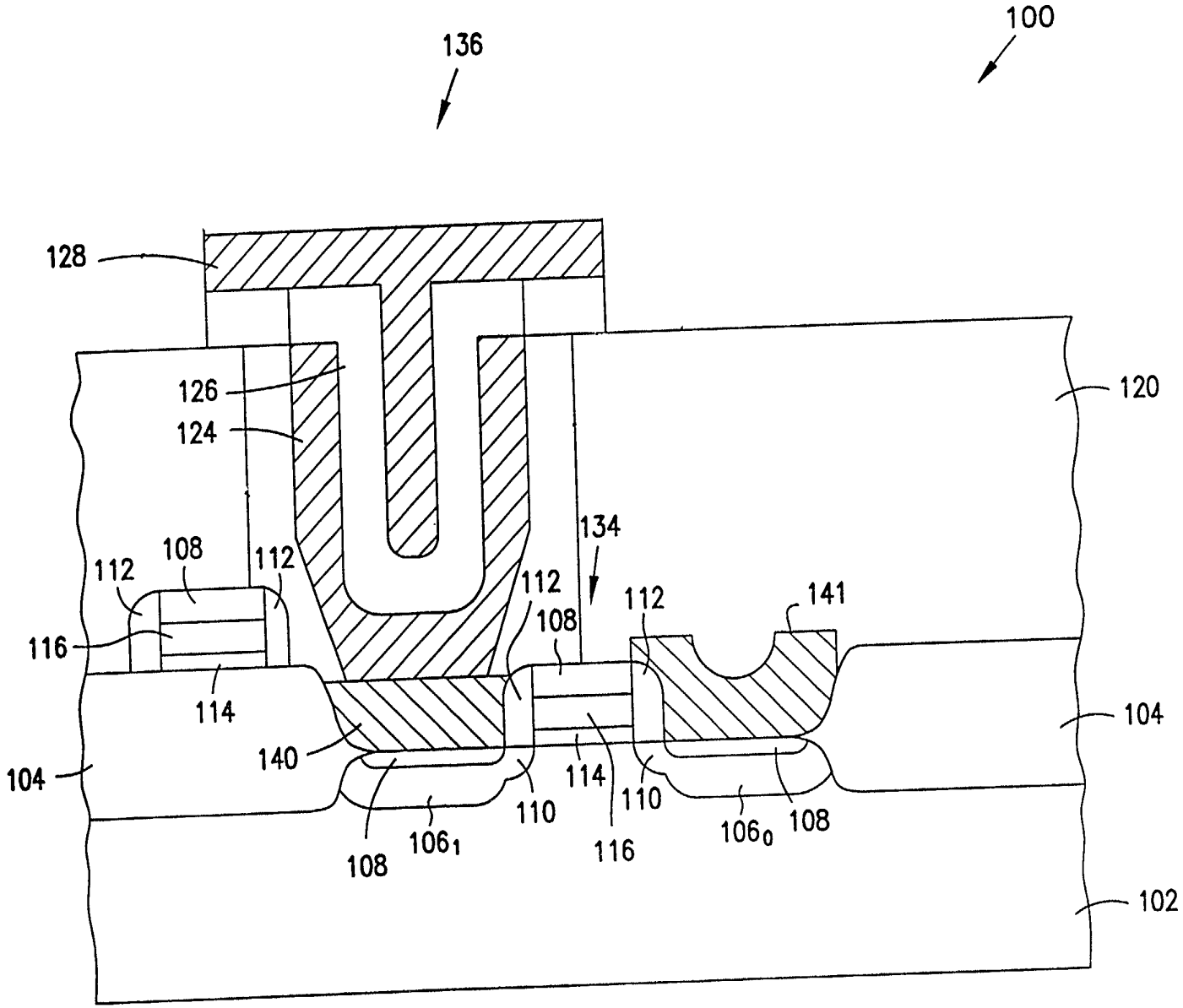

FIG. 1

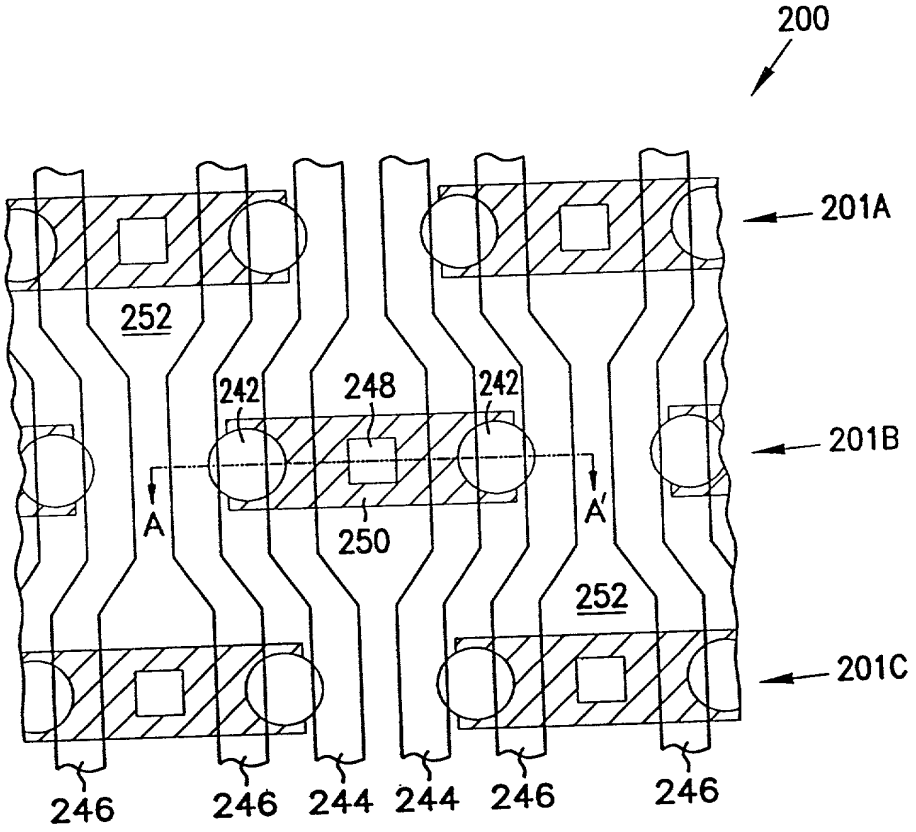
200
201A
252
242
248
242
201B
A
A'
250
252
201C
246
246
244
244
246
246

FIG. 2

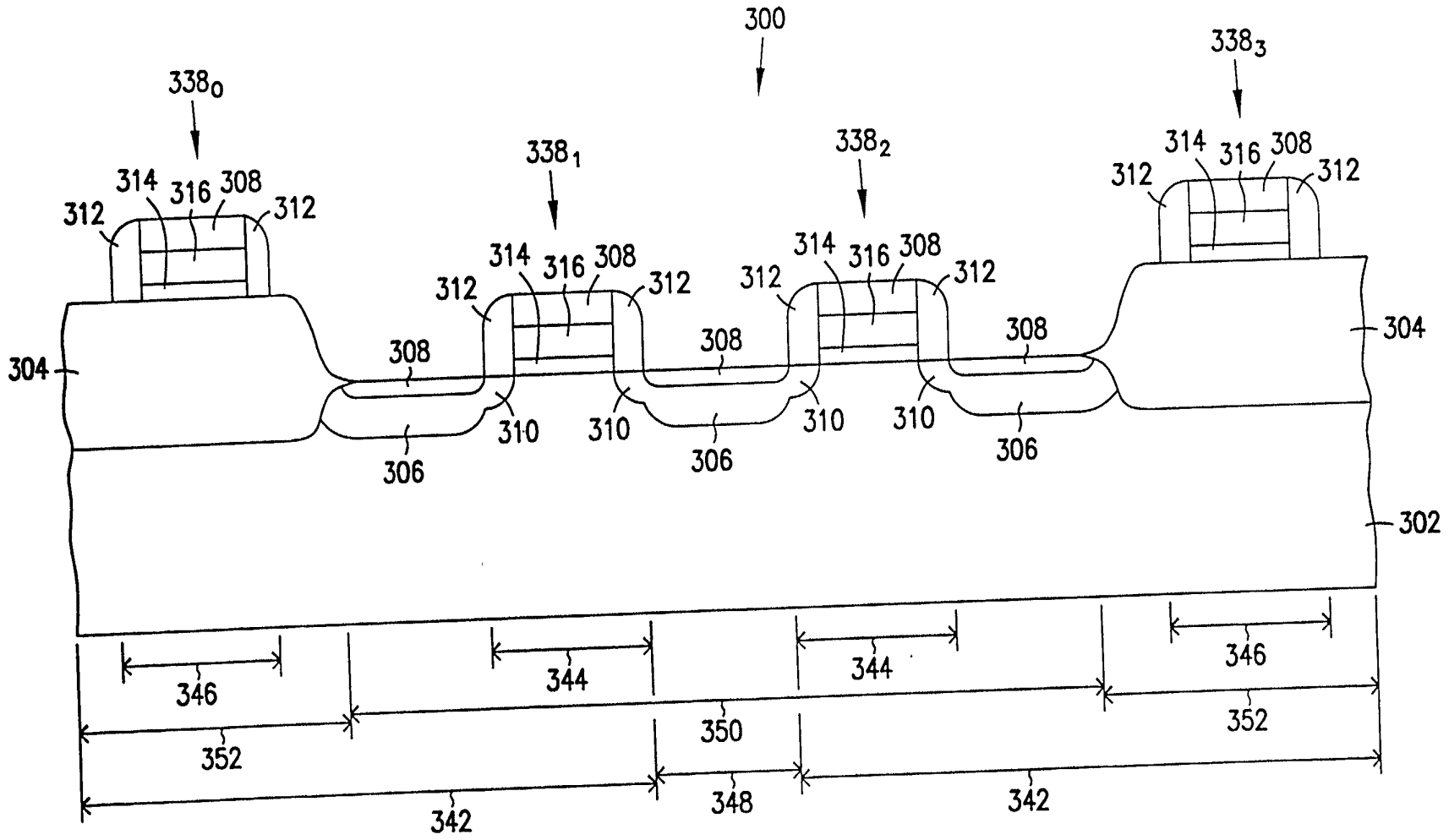

FIG. 3A

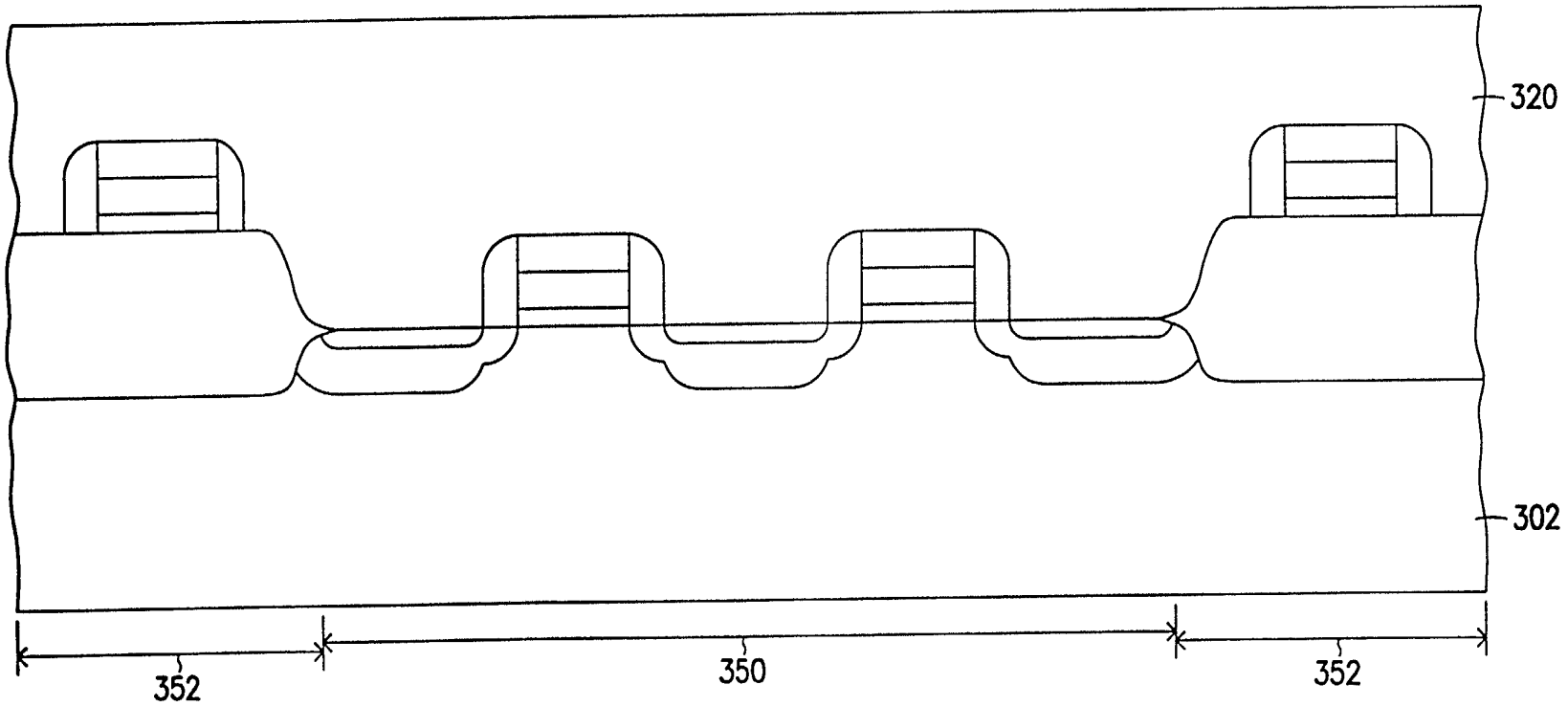

FIG. 3B

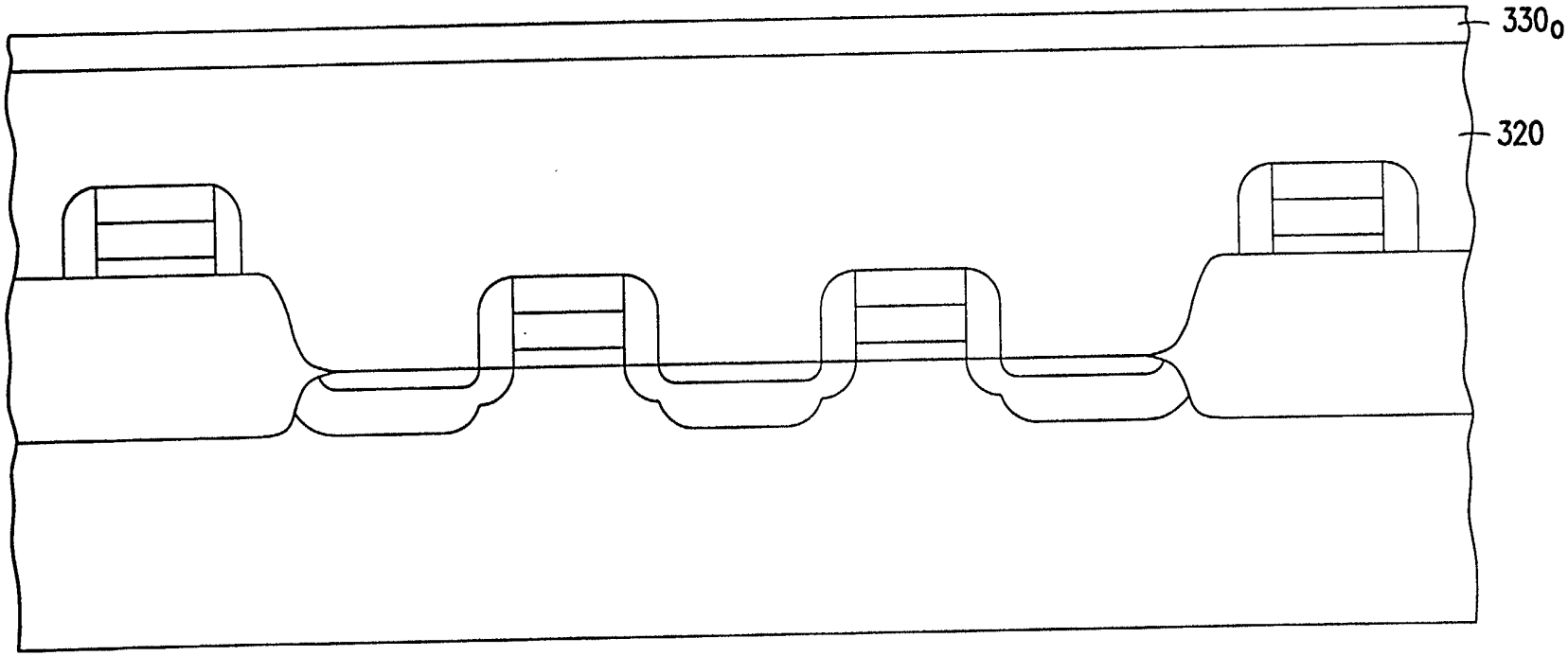

FIG. 3C

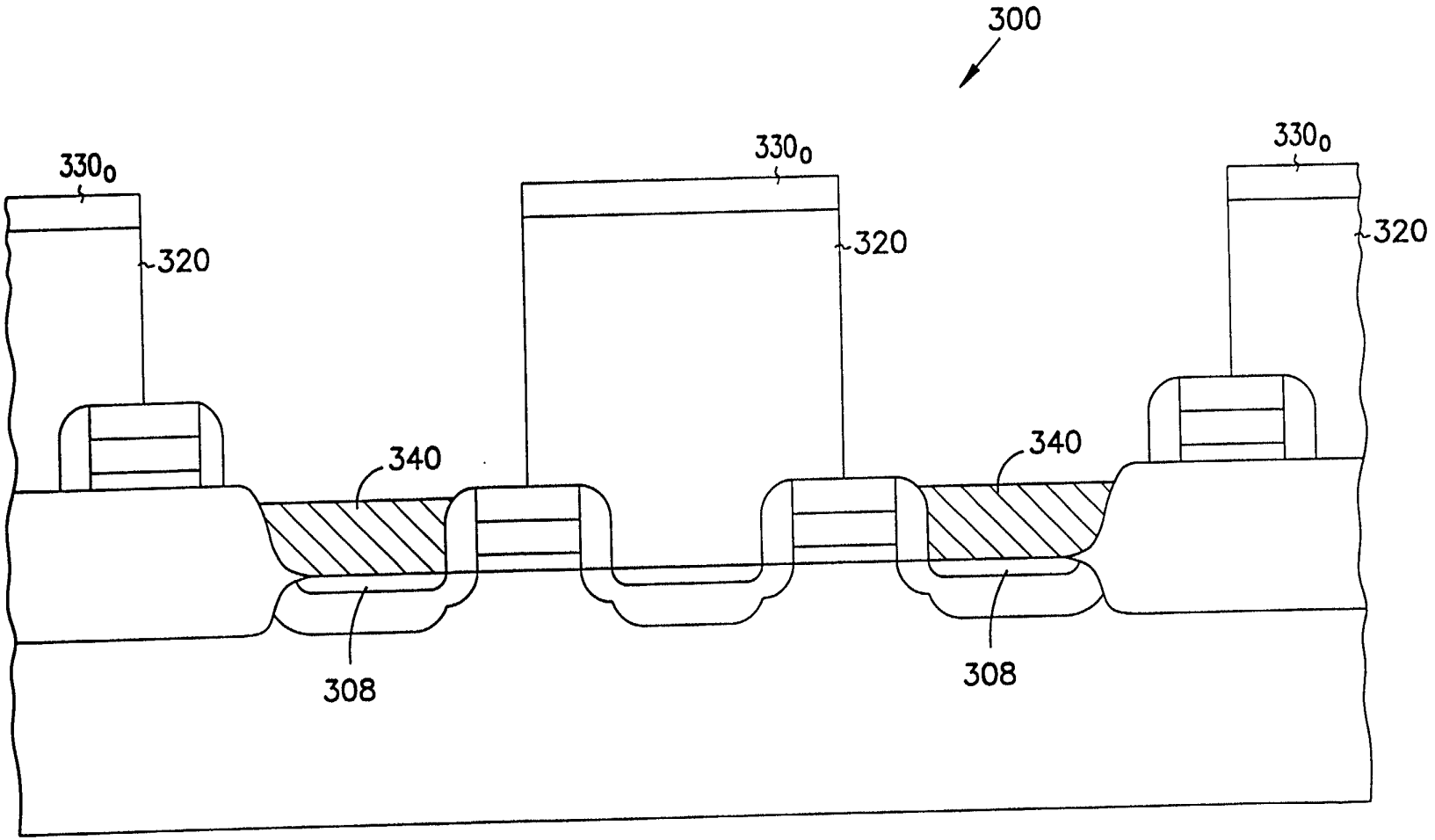

FIG. 3D

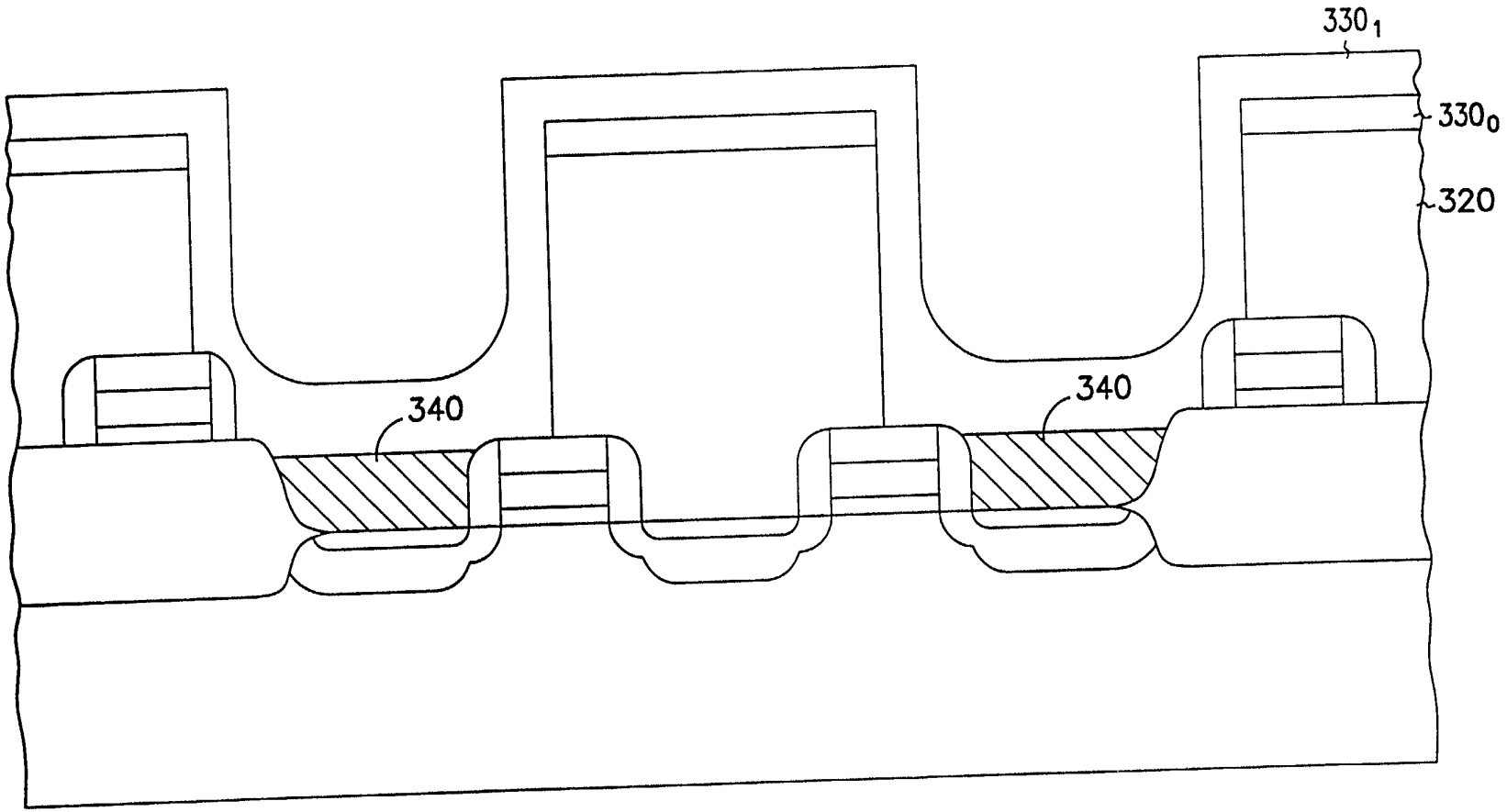

FIG. 3E

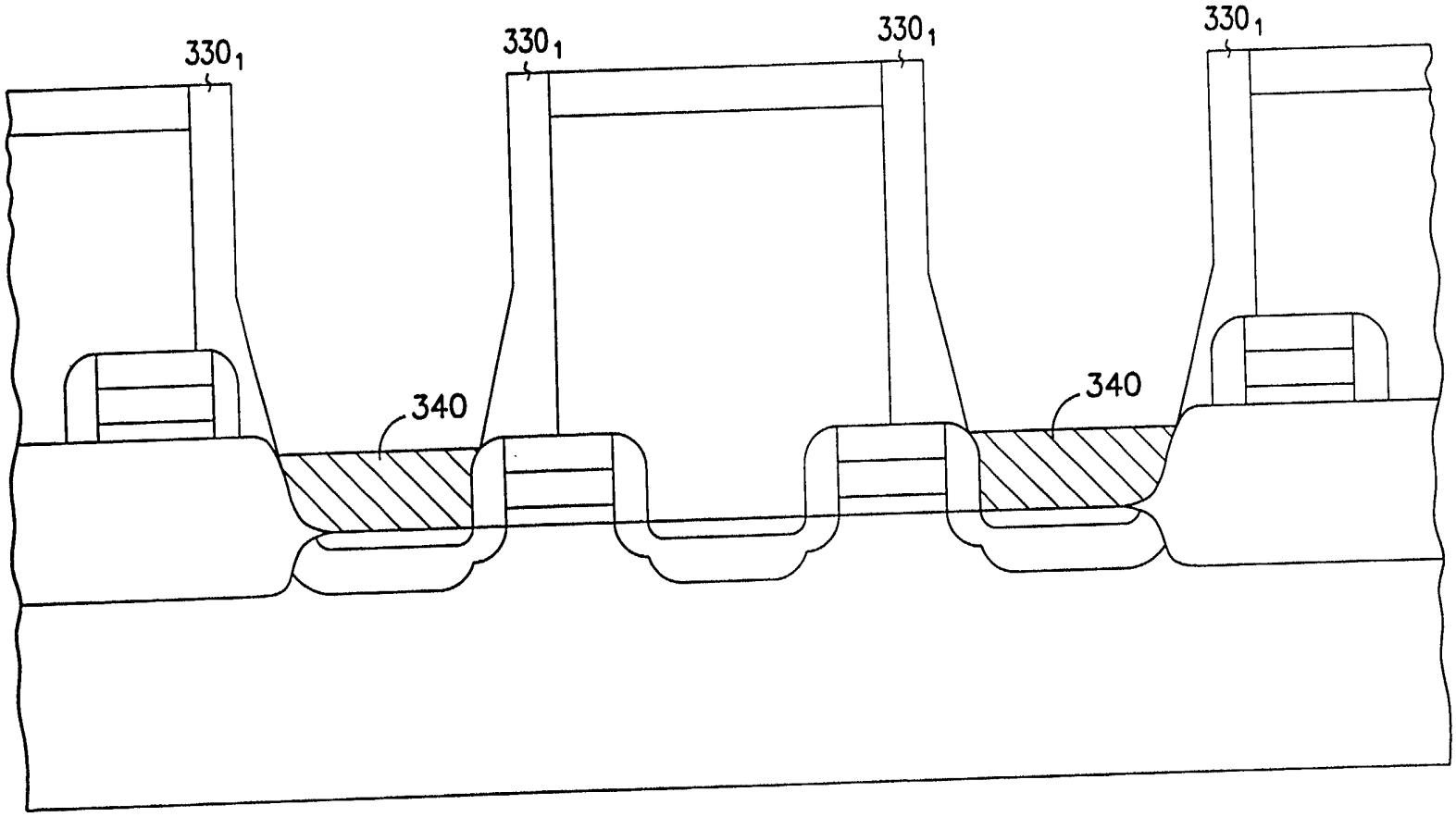

FIG. 3F

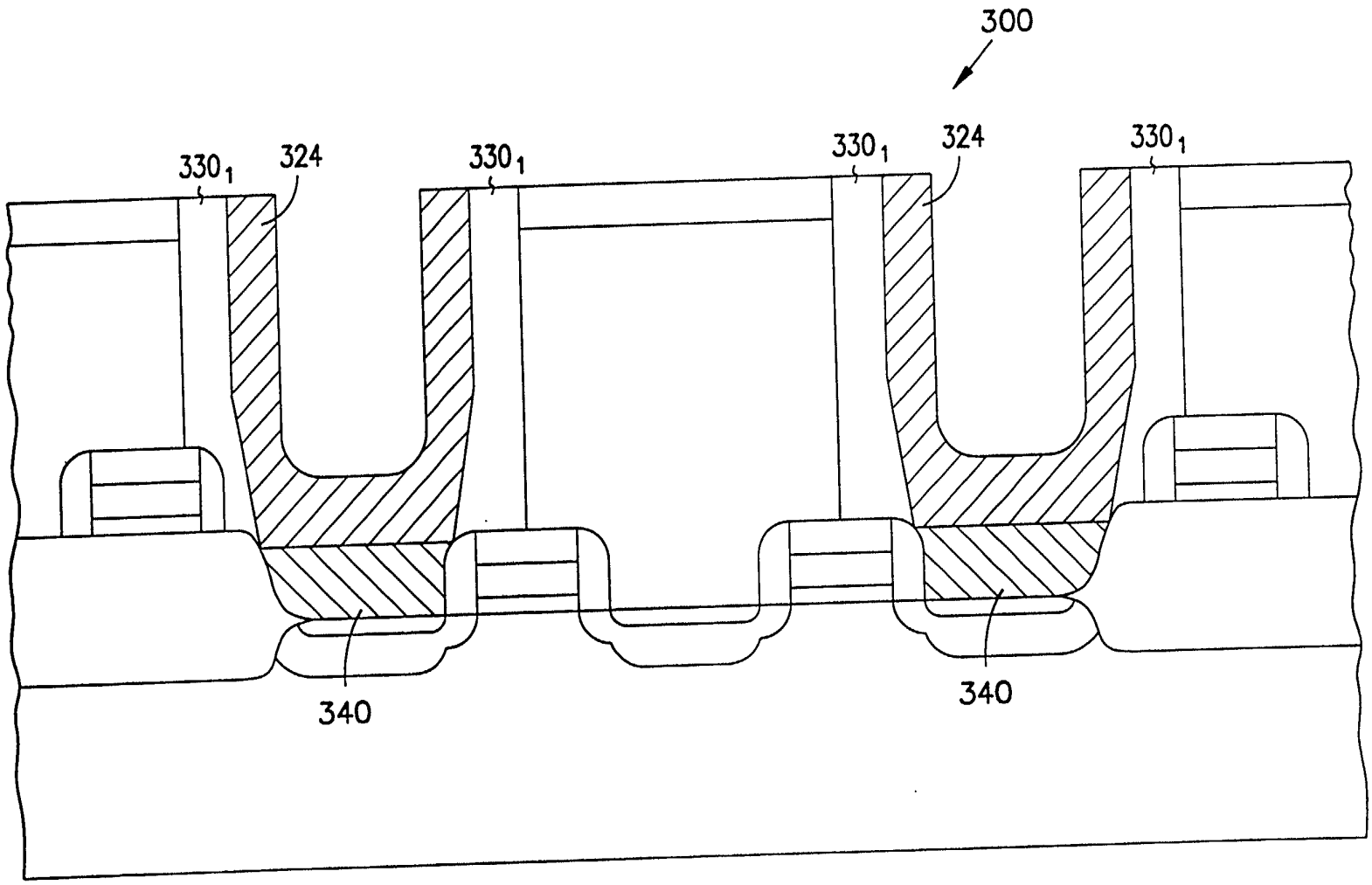

FIG. 3G

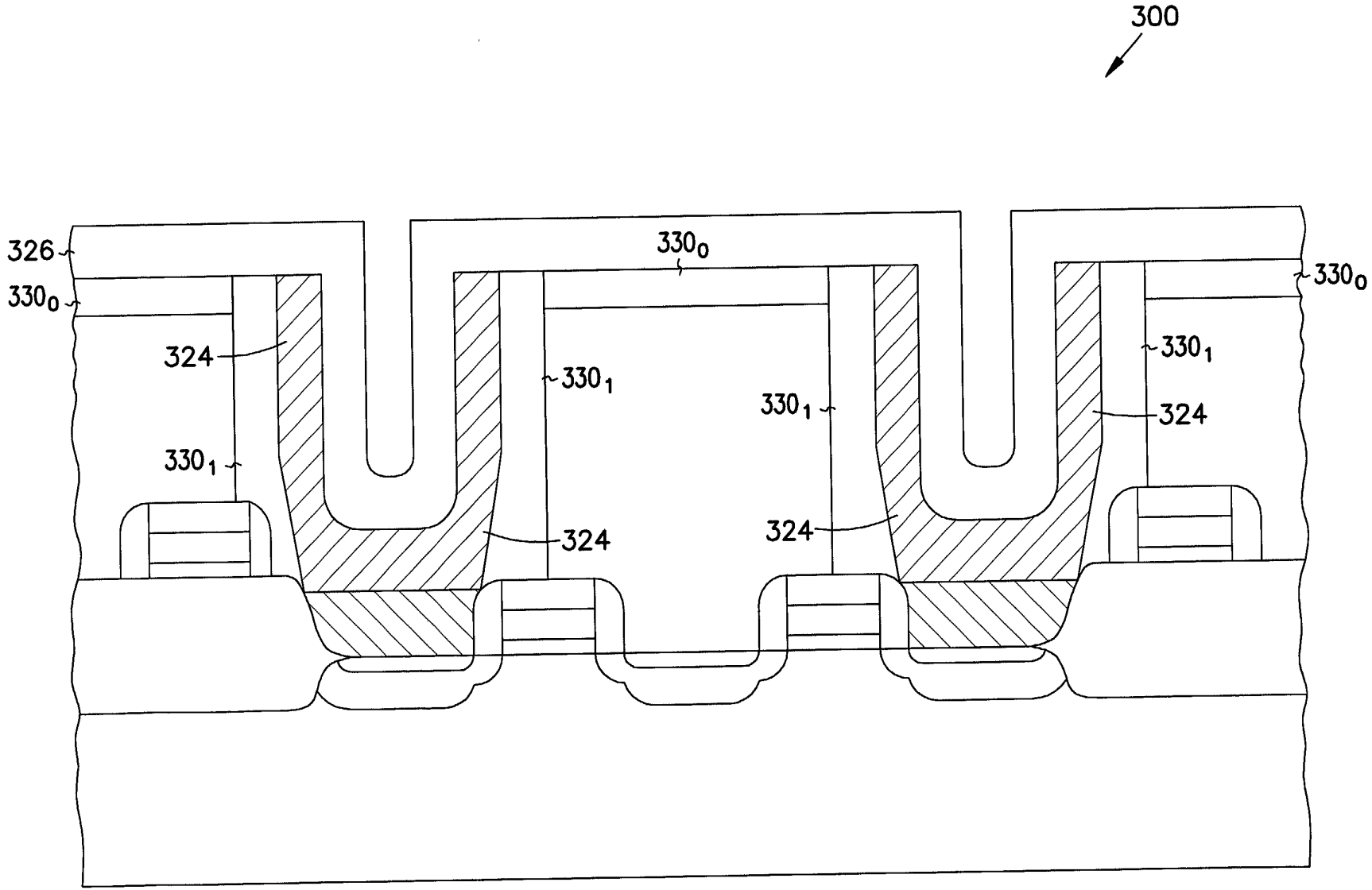

FIG. 3H

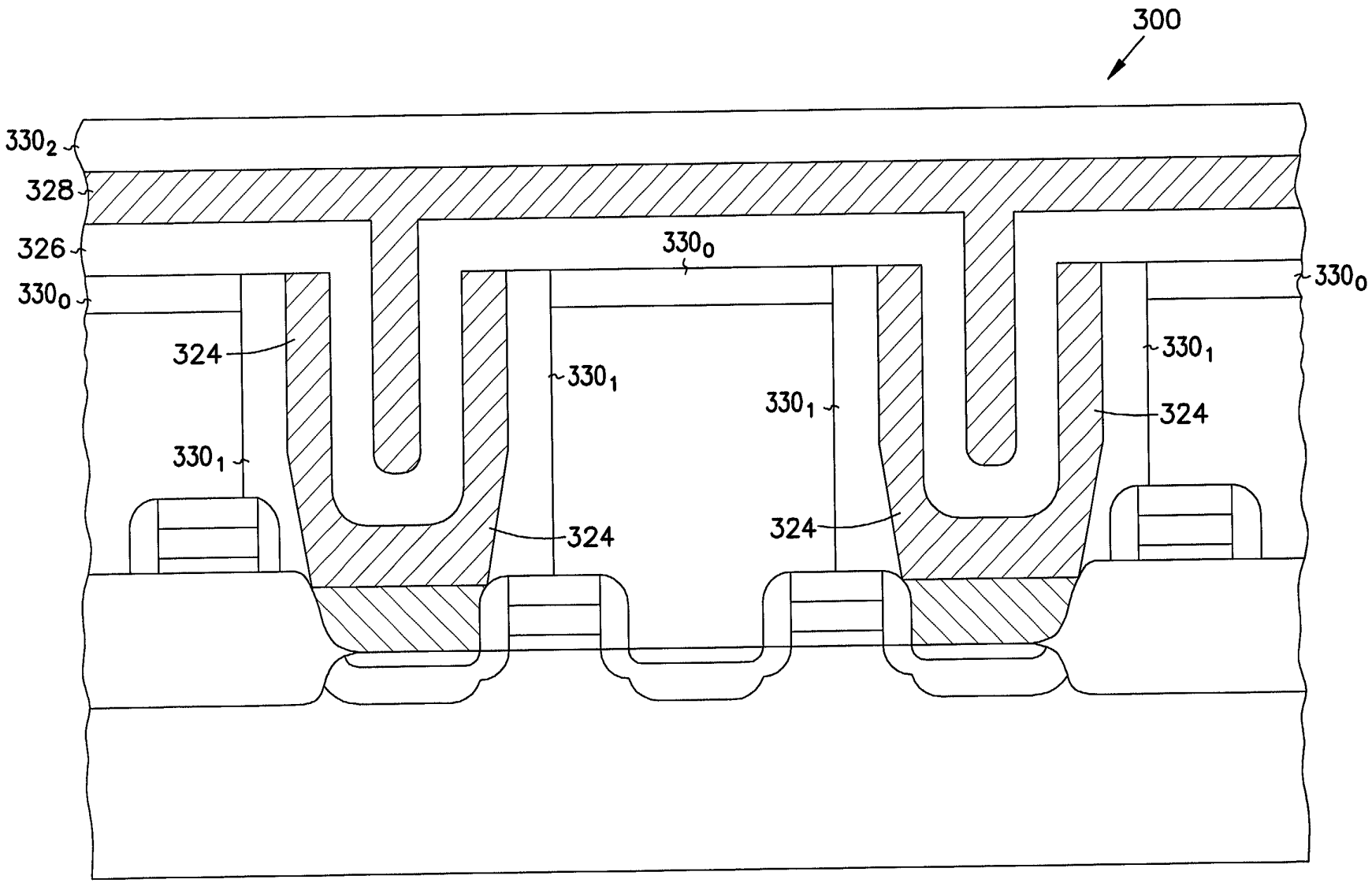

FIG. 31

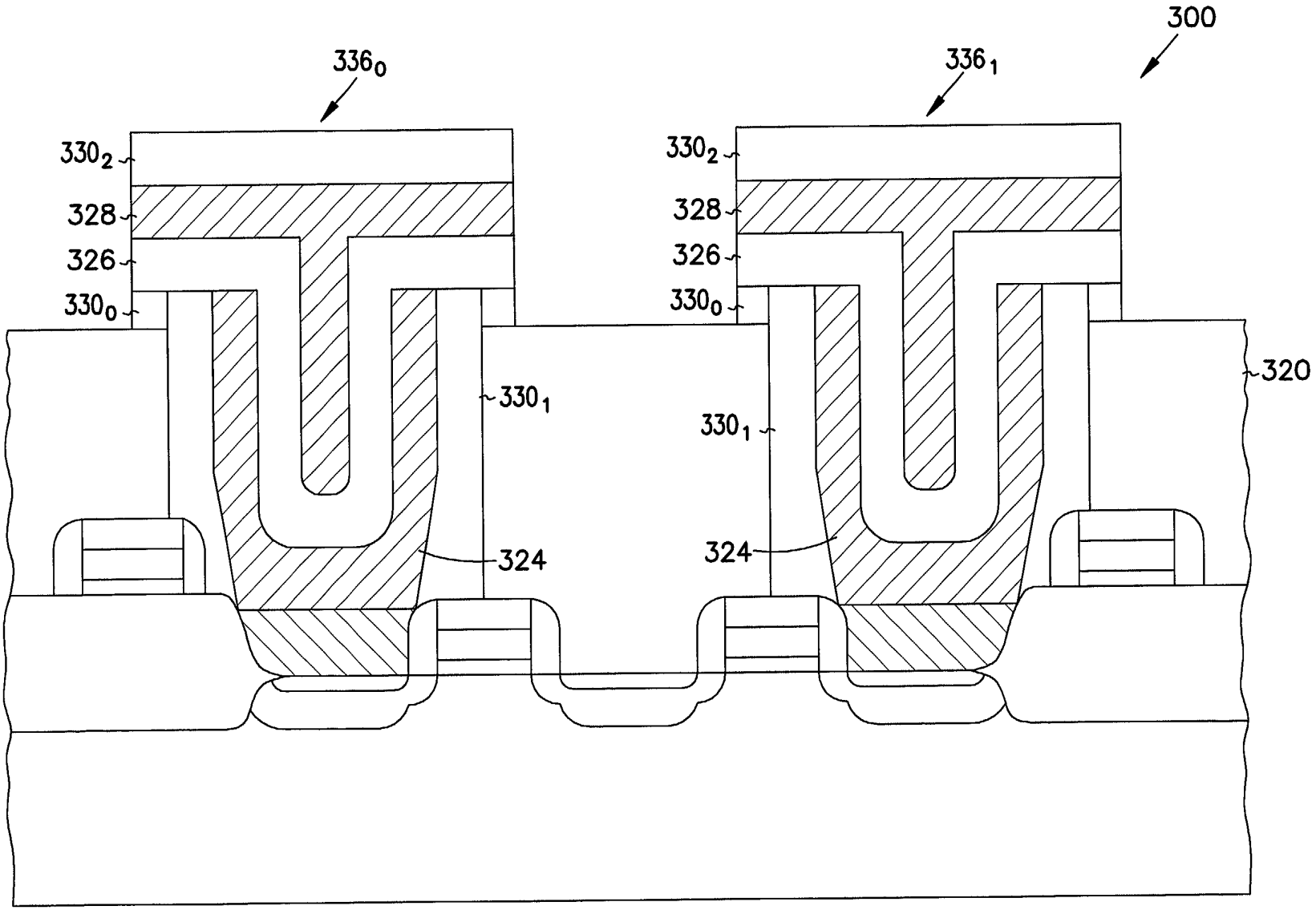

FIG. 3J

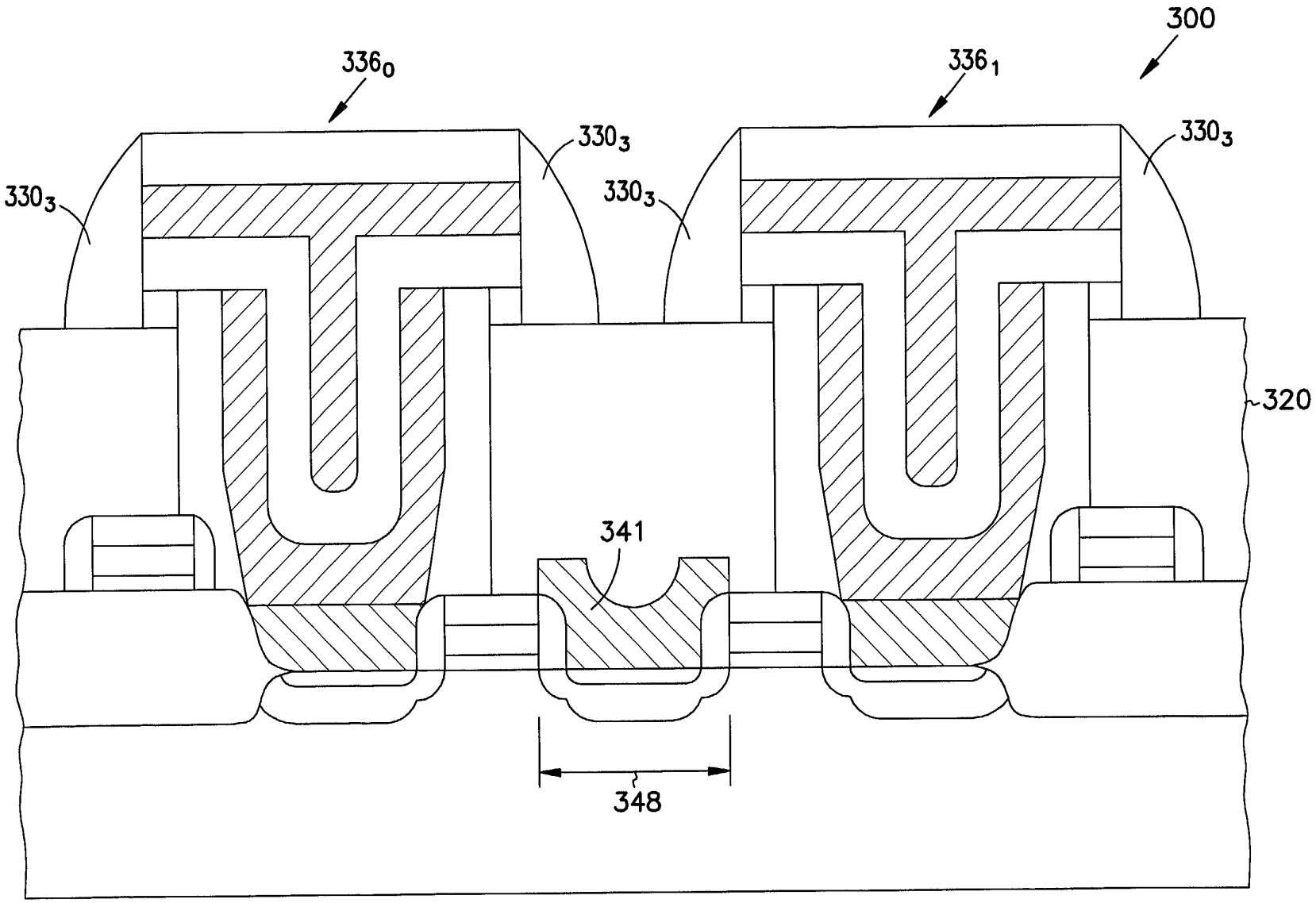

FIG. 3K

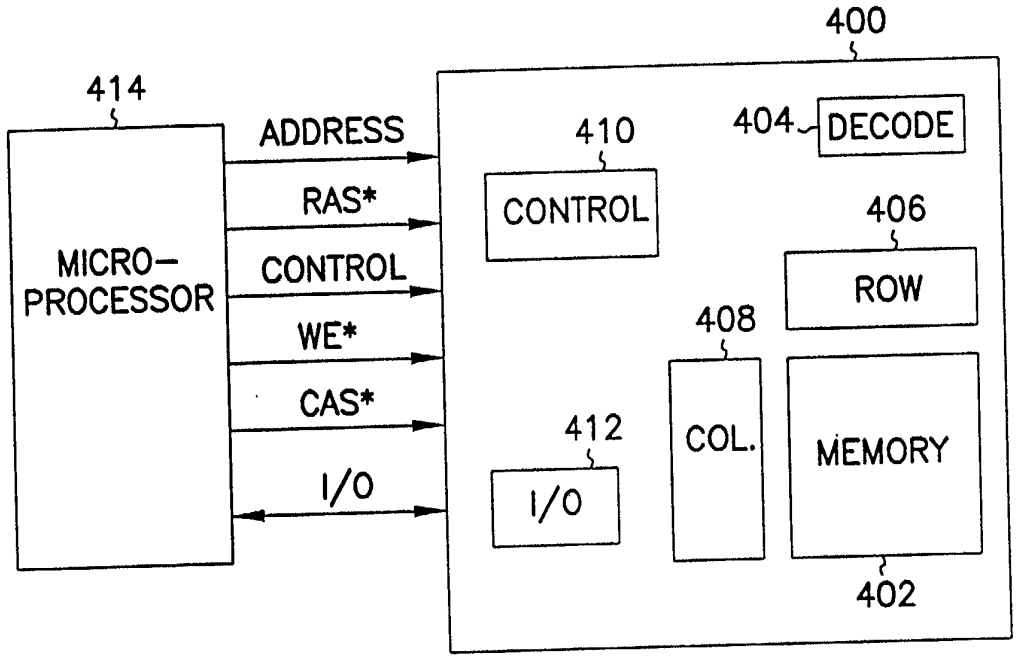

FIG. 4

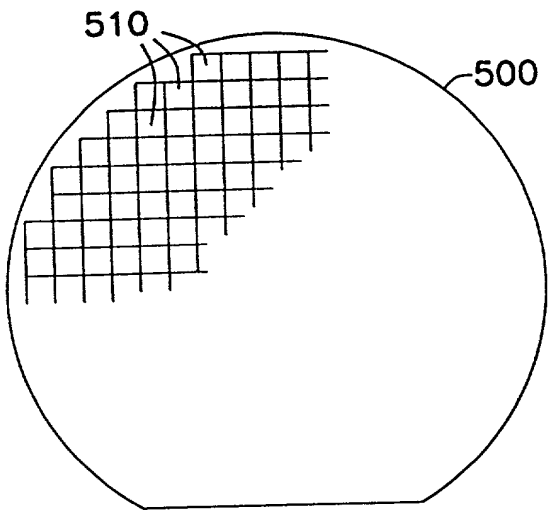

FIG. 5

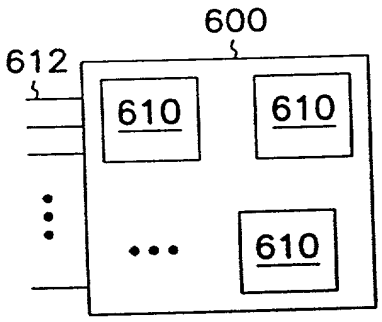

FIG. 6

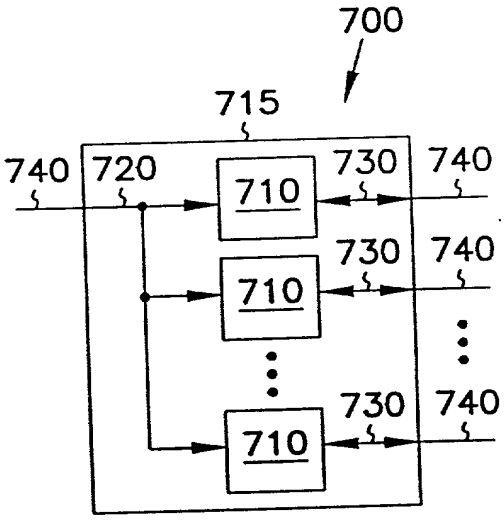

FIG. 7

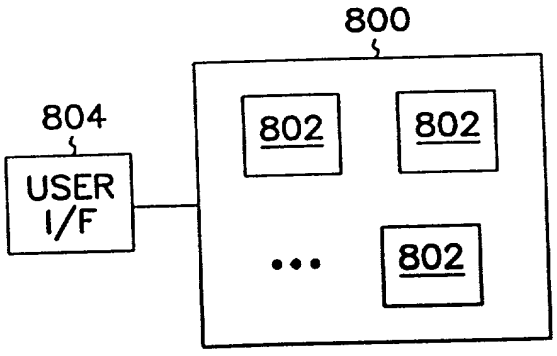

FIG. 8

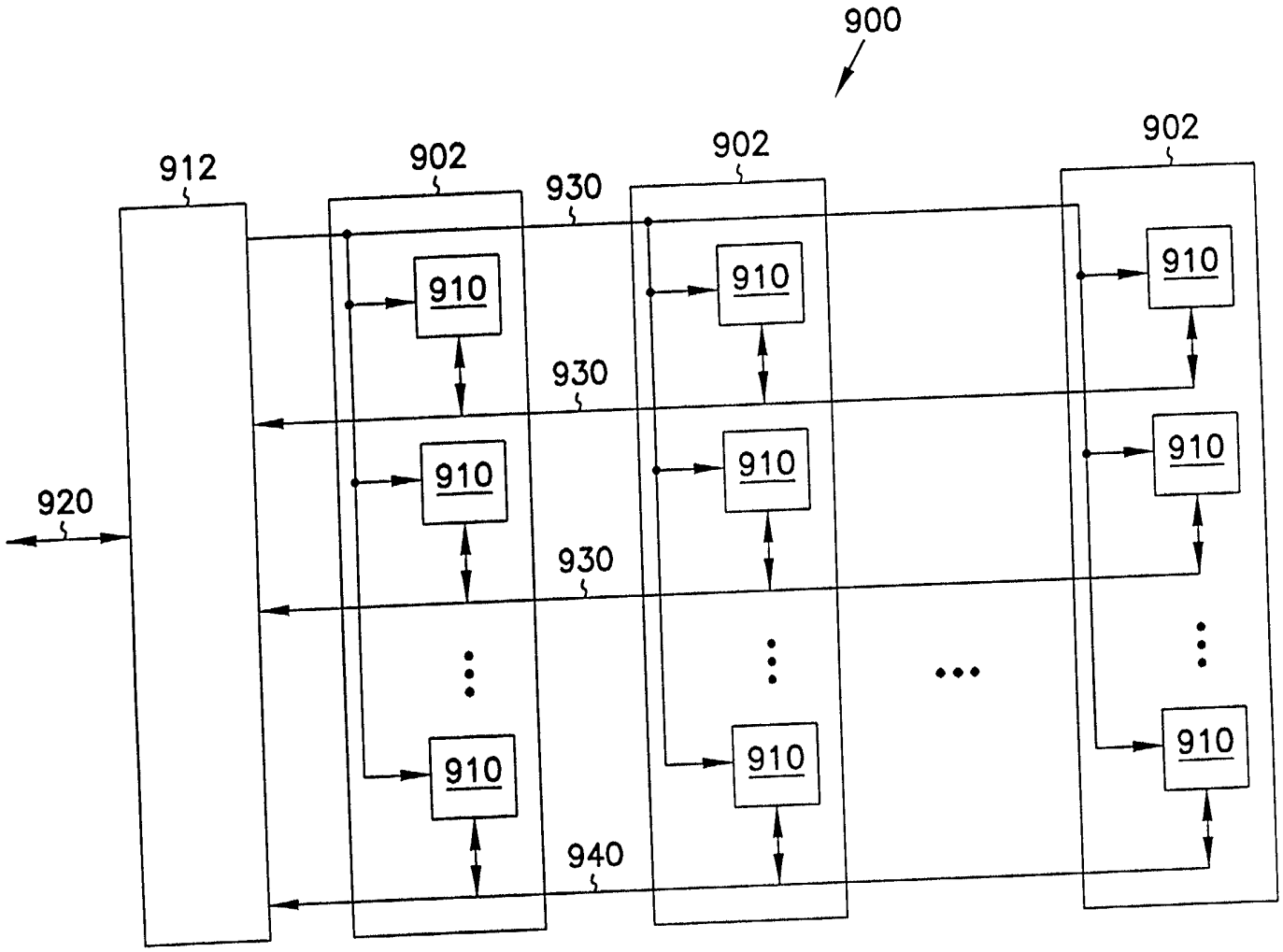

FIG. 9

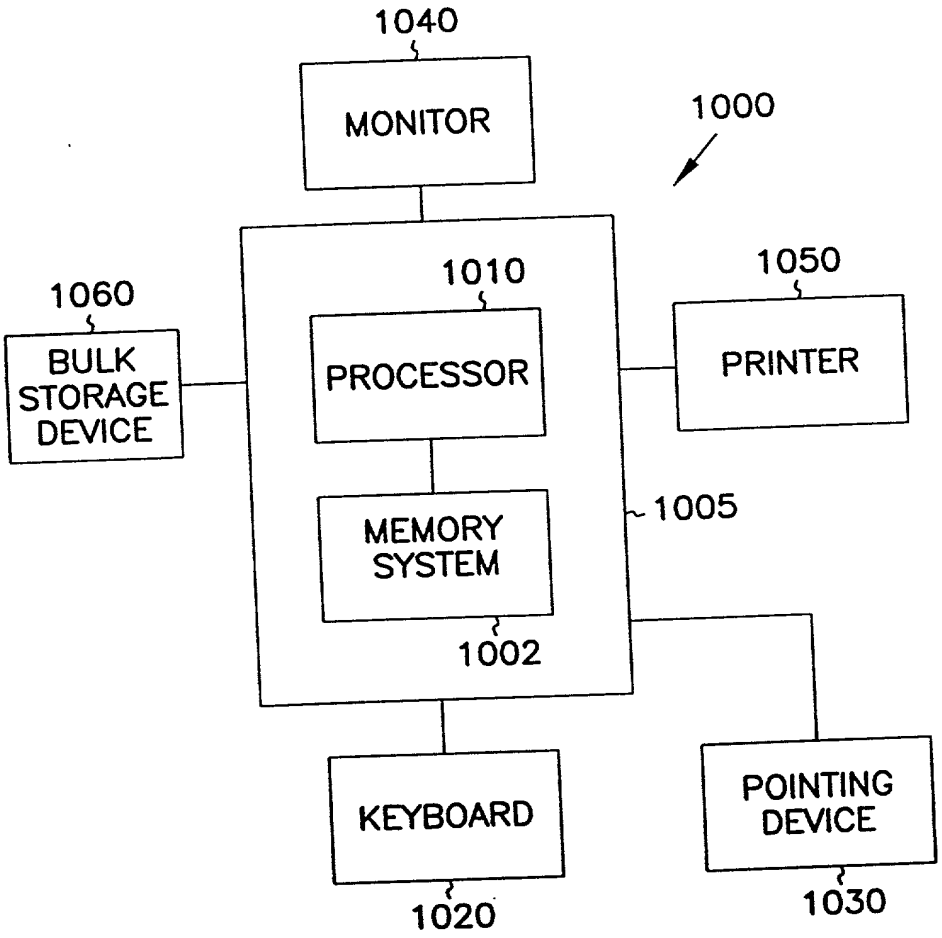
1040
MONITOR
1000
1010
1060
1050
BULK STORAGE DEVICE
PROCESSOR
PRINTER
MEMORY SYSTEM
1005
1002
KEYBOARD
POINTING DEVICE
1020
1030

FIG. 10

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

DECLARATION FOR PATENT APPLICATION

As a below named inventor I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first an joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS .

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application.

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Boise, ID 83706

Signature: Cem Basceri Date: 6-12-00
Cem Basceri

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Boise, ID 83716

Signature: Date: 6/12/00
Vishnu K. Agarwal

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Kuna, ID 83634

Signature: Dan Gealy Date: 6/12/00
Dan Gealy

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) it refutes, or is inconsistent with, a position the applicant takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Cem Basceri et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 303.695US1	
Title:	STRUCTURES AND METHODS FOR ENHANCING CAPACITORS IN INTEGRATED CIRCUITS		

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment attached hereto, hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A., listed as follows:

Anglin, J. Michael	Reg. No. 24,916	Jurkovich, Patti J.	Reg. No. 44,813	Nelson, Albin J.	Reg. No. 28,650
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Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Padys, Danny J.	Reg. No. 35,635
Brennan, Leoniede M.	Reg. No. 35,832	Kluth, Daniel J.	Reg. No. 32,146	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Lacy, Rodney L.	Reg. No. 41,136	Perdok, Monique M.	Reg. No. 42,989
Brooks, Edward J., III	Reg. No. 40,925	Lemaire, Charles A.	Reg. No. 36,198	Prout, William F.	Reg. No. 33,995
Chu, Dinh C.P.	Reg. No. 41,676	LeMoine, Dana B.	Reg. No 40,062	Schumm, Sherry W.	Reg. No. 39,422
Clark, Barbara J.	Reg. No. 38,107	Lundberg, Steven W.	Reg. No. 30,568	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. 44,639	Mack, Lisa K.	Reg. No. 42,825	Smith, Michael G.	Reg. No. 45,368
Drake, Eduardo E.	Reg. No. 40,594	Maeyaert, Paul L.	Reg. No. 40,076	Speier, Gary J.	Reg. No. 45,458
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Steffey, Charles E.	Reg. No. 25,179
Fordenbacher, Paul J.	Reg. No. 42,546	Malen, Peter L.	Reg. No. 44,894	Terry, Kathleen R.	Reg. No. 31,884
Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271	Tong, Viet V.	Reg. No. 45,416
Gamon, Owen J.	Reg. No. 36,143	McCrackin, Ann M.	Reg. No. 42,858	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	Nama, Kash	Reg. No. 44,255	Woessner, Warren D.	Reg. No. 30,440
Huebsch, Joseph C.	Reg. No. 42,673				

and also attorneys Michael L. Lynch (Reg. No. 30,871) and Lia M. Pappas (Reg. No. 34,095) of Micron Technology, Inc., as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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Dated: 6-13-'00

MICRON TECHNOLOGY, INC.

By: _____

Name: Michael L. Lynch

Title: Chief Patent Counsel